

Customer No.: 31561
Docket No.: 10958-US-PA
Application No.: 10/604,651

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-28. Specifically, the Office Action rejected claims 1, 12, 20-28 under 35 U.S.C. 102(e), as being anticipated by Takayama (U.S. 6,610,142). The Office Action also rejected claims 1-28 under 35 U.S.C. 103(a) as being unpatentable over Takayama in view of Jen (JJAP Part 2: Letters 1991, 33(7B), L997-L979) and Luan (Jour. Of Appl. Phys. 1990, 68(7), 3445-3450).

Applicants have amended claims 1, 10 to overcome the rejection. After entry of the foregoing amendments, claims 1-28 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants deem there is a mistake in the 102(e) rejection of claims 1, 12, 20-28. This is because claims 12, 20-28 are dependent on claim 10, but claim 10 is rejected under the 103(a).

Applicants respectfully traverse the 102(e) rejection of claims 1, 12, 20-28 because Takayama (U.S. 6,610,142) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is

Customer No.: 31561
Docket No.: 10958-US-PA
Application No.: 10/604,651

contained in the claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related a method of forming a low temperature polysilicon thin film transistor as claims 1 and 10 recite:

Claim 1. A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:

forming an amorphous silicon layer over a substrate;
performing a plasma treatment to the amorphous silicon layer;
transforming the amorphous silicon layer into a polysilicon layer;
 patterning the polysilicon layer to form a plurality of island polysilicon layers;
 forming a channel region and a doped source/drain region on each side of the channel region in each island polysilicon layer; and
 forming a gate over each channel region.

Claim 10. A method of forming a low temperature polysilicon thin film transistor, comprising the steps of:

providing a substrate;
 forming an amorphous silicon layer over the substrate;
performing a plasma treatment to the amorphous silicon layer;
 performing a laser annealing process to transform the amorphous silicon layer into a polysilicon layer;
 patterning the polysilicon layer to form a plurality of island polysilicon layers;
 forming a gate insulation layer over the island polysilicon layers;
 forming a channel region in each island polysilicon layer and a doped source/drain region on each side to the channel regions; and
 forming a gate over the channel regions.

Tokayama fails to disclose that a plasma treatment is performed to the amorphous silicon layer. In Takayama's reference, the plasma treatment is performed to a silicon oxide layer but not to the amorphous silicon layer. In Example 1 of the reference, a thick silicon oxide film is deposited on a substrate, and the resulting silicon oxide film is treated in nitrogen plasma (col. 6,

Customer No.: 31561
Docket No.: 10958-US-PA
Application No.: 10/604,651

lines 44-46). In Example 2 of the reference, as shown in Fig. 2A, a silicon oxide film 22 is deposited on a substrate 21 and a photoresist 24 is formed on the silicon oxide film 22. Then, as shown in Fig. 2B, the entire substrate is exposed to nitrogen plasma to performed plasma treatment on the exposed portion 23 of the oxide film base (col. 8, line 63~col. 9, line 3). In Example 3 of the reference, as shown in Fig. 3A, a silicon oxide film 31 is deposited on a substrate 30, and then a plasma treatment is performed. After the plasma treatment, an amorphous silicon film is deposited (col. 9, line 67~col. 10, line 20). Similarly, in Examples 4 and 5, the plasma treatment is performed on the silicon oxide film 41 or 22, and then an amorphous silicon film 43 or 25 is deposited. Therefore, Takayama fails to disclose that a plasma treatment is performed to the amorphous silicon layer. Takayama does not teach every element recited in claims 1, 10.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 10 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-28 patently define over the prior art as well.

Applicants respectfully traverse the rejection of claims 1-28 under 35 U.S.C. 103(a) as being unpatentable over Takayama in view of Jen (JJAP Part 2: Letters 1991, 33(7B), L997-L979) and Luan (Jour. Of Appl. Phys. 1990, 68(7), 3445-3450)) because a prima facie case of obviousness has not been established by the Office Action.

Customer No.: 31561
Docket No.:10958-US-PA
Application No.: 10/604,651

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Applicants submit that, as disclosed above, Takayama fail to teach or suggest each and every element of claims 1, 10, from which claims 2-9, 11-28 depend.

In Lurn's reference, the NH₃ plasma treatment is performed to a gate nitride layer. The NH₃ plasma treatment immediately following SiNx deposition. In Jen's reference, N₂O plasma is used to treat the deposited SiOxNy/SiNx gate insulators. Therefore, both Lurn and Jen fail to teach or suggest that a plasma treatment is performed to the amorphous silicon layer. Lurn and Jen cannot cure the deficiencies of Takayama. Therefore, independent claims 1 and 10 are patentable over Takayama, Lurn and Jen. For at the least the same reasons, their dependent claims 2-9, 11-28 are also be patentable.

Customer No.: 31561
Docket No.: 10958-US-PA
Application No.: 10/604,651

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : July 20, 2005



Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Uaa@jcipgroup.com.tw